Leakage Power Reduction Techniques Revisited in a CMOS Inverter Circuit at Deep Sub-micrometer CMOS Technology

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***Abstract*- As CMOS Technology is aiming at miniaturization of MOS devices, a trend of increase in the static power consumption is being observed. The main sources of static power consumption are sub-threshold current and gate oxide leakage current. In this work, we discuss the major sources of power consumption, various techniques to reduce leakage power and their trade-offs in a CMOS inverter logic circuit at 90nm. Three most popular leakage current reduction techniques are studied with respect to a conventional inverter circuit. It is seen that the main trade-off is between the area and the static leakage current. This paper aims to reduce the static power dissipation with a small compromise in area.**

***Index Terms*- Domino Logic, Dynamic Power, Gate Oxide Leakage, Sleepy Method, Static Power, Stack Effect, Sub-threshold Leakage, Threshold Voltage.**

I. Introduction

Power dissipation is an important parameter in the development of electronic devices. The latest technology often tends to bend to the demand for compact and portable devices but when size decreases leakage power due to leakage currents increases. Our main aim is to minimize the leakage currents without any compromise in size.

Power dissipation is of two types, dynamic and static. Dynamic power dissipation occurs in the circuit mainly due to charging and discharging while static power dissipation is due to the leakage current, Eq. 1 [1][2]. For reducing the dynamic power consumption, devices are subjected to scaling which in turn reduces the threshold voltage causing increase in leakage. This complementary dependence of static and dynamic power is a major issue observed in the VLSI circuits.

Based on the report from International Technology Roadmap for Semiconductors (ITRS), the sub-threshold leakage power dissipation of a chip may exceed dynamic power dissipation at the 65nm feature size [1]. So we are in need of techniques and methods to describe the reduction in leakage. Different methods are applied depending on the requirements of the application to reduce leakage. For reduction of leakage power at circuit level various techniques like stack effect, sleepy method, sleepy stack, sleep switch domino logic, multiple threshold technology etc are used. The leakage occurs when the transistor is in the off state or stand- by mode.

$$Power_{static} = V_{dd} \times I_{leakage} \quad (1)$$

Where $Power_{static}$ = static power, V_{dd} = supply voltage and $I_{leakage}$ =total leakage current.

Leakage current has five components [3] [4],

1. Reverse biased p-n junction current
2. Sub-threshold leakage current
3. Gate-Induced Drain leakage current
4. Punch through current
5. Gate Tunneling current

The main source of leakage power is the sub-threshold current and oxide leakage current, Eq.2 [5] which depends mainly on threshold voltage.

$$I_{leakage} = I_{sub} + I_{ox} \quad (2)$$

Where I_{sub}= Sub-threshold leakage current and I_{ox}= oxide leakage current. Figure 1 shows these two leakage current components in a CMOS inverter circuit.

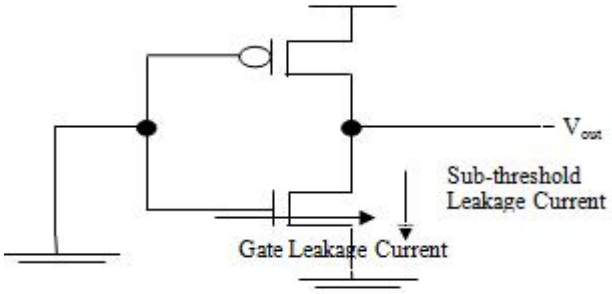

Figure 1. Leakage Current Components in a CMOS Inverter

II. Leakage Current Mechanisms: A Review

According to the various research papers, we are concerned with sub-threshold conduction and gate oxide leakage. Before we go further into the methods, let us analyze the above said leakage currents and their dependence on the various parameters involved.

A. Sub-Threshold Leakage Current

Sub-Threshold is the leakage current, Eq.3 [6] that flows between source and drain of MOSFET transistor during $V_{gs} < V_t$ [2] [6], where V_{gs} is the gate to source voltage and V_t is the threshold voltage. Sub-threshold region is also referred to as weak inversion region [3] [7]. The sub-threshold conduction is dependent on V_t which gets reduced when supply voltage is scaled [8]. This reduction in V_t results in the exponential increase of sub-threshold leakage current and will be more

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significant when MOSFET shrink in size.

$$I_{sub} = KW e^{\left(\frac{Vgs-Vt}{nvt}\right)}\left(1 - e^{-V/vt}\right) \quad (3)$$

Where $K=\mu C_{ox} V_t^2/L$ with μ=mobility, Cox= oxide capacitance and L= length of gate, W= width of the gate, n= sub-threshold swing coefficient, V= drain to source voltage and vt= thermal voltage.

Two main techniques used to reduce the sub-threshold current are by turning off the supply voltage, which results in loss of state and by increasing V_t, which causes loss of performance as low threshold is preferred for good driving capability [3]. Sub-threshold current is also affected by body effect which increases the threshold voltage as given by Eq. 4 [6]

$$V_t \approx V_{t0} + \gamma V_{sb} - \eta V_{ds} \quad (4)$$

Where γ = body effect coefficient, η = DIBL coefficient, V_{sb}= source-body voltage, V_{ds}=drain to source voltage and V_{t0} = threshold voltage when there is no body effect.

This leakage is exponentially dependent on junction temperature, V_{gs}, V_{ds} and V_t. Significant portion of threshold leakage is also due to Drain induced Barrier Lowering (DIBL).

In CMOS Technology, devices were reduced in size to increase their density on chips leading to higher power. Our major concern when we reduce the size of a device is the leakage current especially the sub-threshold current. In sub-threshold region, drain current behaves similar to the exponentially increasing current of forward biased diode as given in Eq. 5 [1].

$$I_d \propto e^{\left(\frac{V_{gs}}{nV_t}\right)} \quad (5)$$

Maximum sub-threshold leakage occurs when a transistor operates in cut-off region [6].

B. Gate Oxide Power Leakage

Gate Leakage, Eq.6 [5] is due to both gate oxide tunneling and injection of hot carriers from substrate to gate oxide. Due to scaling down device size, it leads to very thin oxides thus gate current of the order of sub-threshold current flows from channel to gate. This increases the static standby power consumption. By increasing t_{ox} we reduce the I_{ox} as seen from Eq.6 but it degrades the performance of transistor.

$$I_{ox} = KW(V/t_{ox})^2 e^{-\alpha t_{ox}/V} \quad (6)$$

Where t_{ox}= oxide thickness

To avoid short channel effects and to improve driving capabilities, t_{ox} must decrease proportionally with scaling [5]. This limits scaling of oxide thickness. Therefore a trade-off exists between oxide thickness and gate leakage

Tunneling Mechanism for Gate Leakage

i. Fowler Nordheim Tunneling-It is the dominant current tunneling mechanism especially for thick oxides. Electrons tunnel through barrier in presence of a high electric field. It is usually observed at high oxide voltage, $V_{ox} > \Phi_b$ (barrier height) [3] [6].

ii. Direct Tunneling-This type of tunneling is common in very thin oxides of $t_{ox} < 4$nm and occurs when $V_{ox} < \Phi_b$. It is dependent on voltage across gate dielectric, thickness of dielectric, tunneling barrier height, effective mass of carriers, and number of free carriers available for tunneling on the MOS electrodes [3][6].

III. Leakage Current Reduction Techniques- A Review

A. Stack Effect

In this method, a single transistor is divided into two transistors of half the size as in Figure 2 [4] [7]. When there are in the off state, the induced reverse biasing between the transistors cause reduction of sub-threshold current [1]. According to reports, it has been found that stacking technique reduces static power dissipation by 9.44% [9].

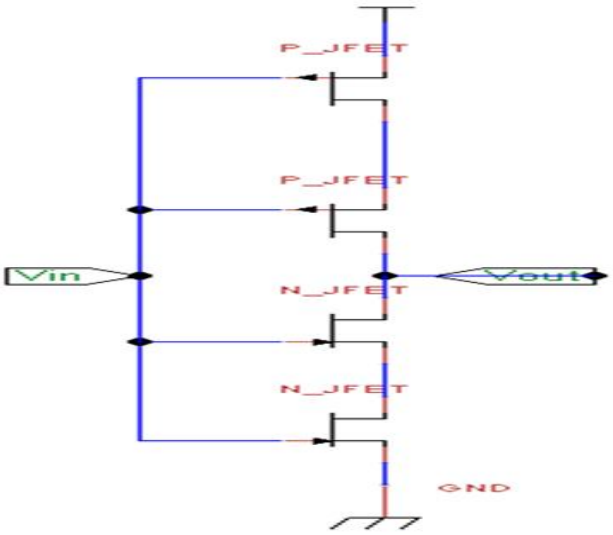

Figure 2. Stacking in inverter

For example we are taking the case of an inverter where two transistors are replaced with four transistors. The positive potential, V_x between the two nMOS cause reduction in sub-threshold leakage as in M1 (nMOS transistor from which output is taken) gate source voltage becomes negative, body source voltage becomes positive and drain to source voltage decreases [2].

B. Sleepy Method

It involves the technique of adding a sleep transistor between pull-up circuit and the supply voltage and between pull-down circuit and ground. They are used to cut-off voltage supply as they turn off at idle state. Sleep mode results in loss of state. One transistor between pull-down and ground can also be used instead of two but this may result in larger power dissipation [2]. In this type of method, a virtual supply voltage and a virtual ground is formed to result in leakage reduction. We can refer the inverter for this technique as a floating inverter as shown in Figure 3.

C. Sleepy Stack

This method is a combination of stack and sleep method where one transistor is divided into two transistors of half

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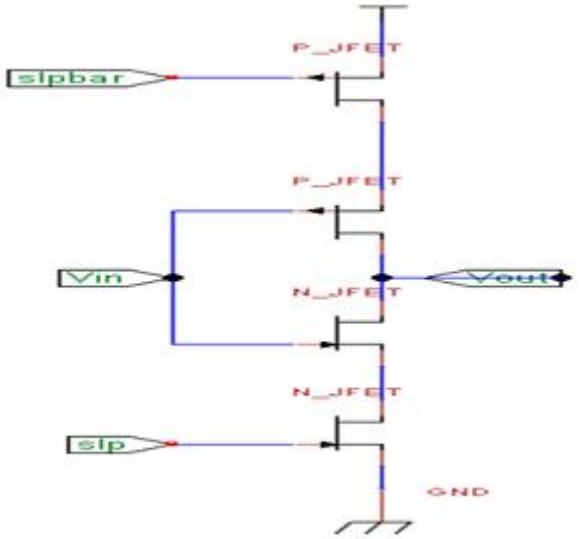

Figure 3. Sleepy Inverter

the size and a sleep transistor is then added parallel to it as in Figure 4 [4][7]. These logic connections results in decrease of resistance which causes decrease in delay. We find that even though this technique results in better leakage reduction technique, it is at the expanse of area [1]. Sleepy stack is better used for low voltage levels to bring about reduction in leakage currents and for state retention [2].

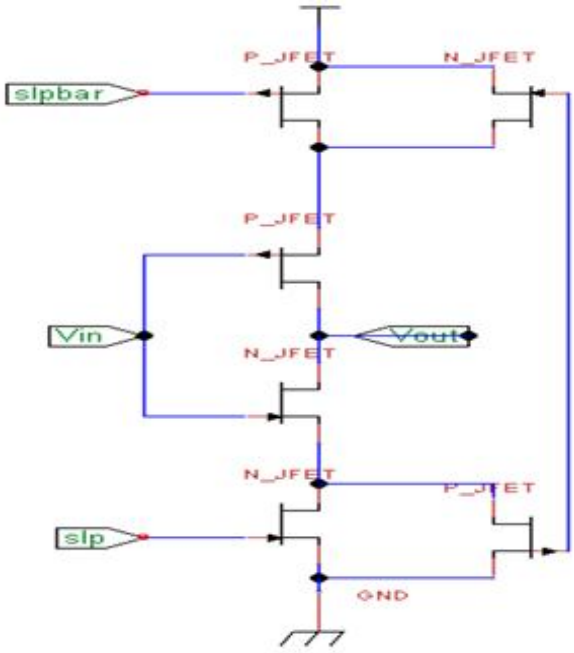

Figure 4. Sleepy Stack

D. Multiple V_t Technology and Other Techniques

In Multiple V_t techniques, two types of thresholds are developed one which is low to reduce dynamic power dissipation while a high V_t reduces the static power dissipation [10]. The Multiple Threshold CMOS (MTCMOS) uses high V_t sleep device in series with low V_t device [4][7] and Dual Threshold CMOS (DTCMOS), uses low V_t transistors in critical path to maintain performance while high V_t transistors used in non-critical path will minimize the leakage currents [8]. Multiple Thresholds are achieved by various methods like multiple gate oxide, multiple channel length, multiple body bias and multiple channels doping which increase V_t to reduce sub-threshold leakage current [3]. Double Gated Dynamic Threshold SOI (DGDT-SOI) [8] [10] and Dual Threshold Transistor Stacking Technique [11] are some similar approaches in this field. In domino logic, techniques proposed for leakage current reduction consists of Leakage Biased Sleep Switch Dual-V_t Domino Logic [12], Dual V_t Footless and Footed Domino Logic and pMOS Pull-up Feedback Transistor, Multiple V_t and Multiple t_{ox} Footed Domino Logic [13]. Novel Sleepy Inverter and State Retention Low Leak Inverter are also popular techniques for leakage reduction [2].

IV. Design Simulation and Analysis

We are revisiting and comparing the stack,sleepy and sleepy stack leakage reduction techniques with conventional inverter in this paper. For conventional inverter circuit and sleepy method, we are using a pMOS and an nMOS transistor with (W/L) ratio of 1.2 while for the stack and sleepy stack the ratio is reduced to 0.6. The various leakage power recorded against the different techniques applied are shown in Figure 5 which shows that stack has the least leakage current while Figure 6 enables us to understand how the leakage power of each techniques vary with voltages from the range of 1V to 2V. We are also studying area on the basis of number of transistors as represented in Figure 7 for leakage reduction techniques and conventional inverter. To measure the stability of the circuit we are measuring the noise margin which is graphically explained in Figure 8. The simulation is done on the tool Cadence Virtuoso in 90nm CMOS technology and the static power for the circuit is calculated by using dc analysis without giving any stimuli to the inverter.

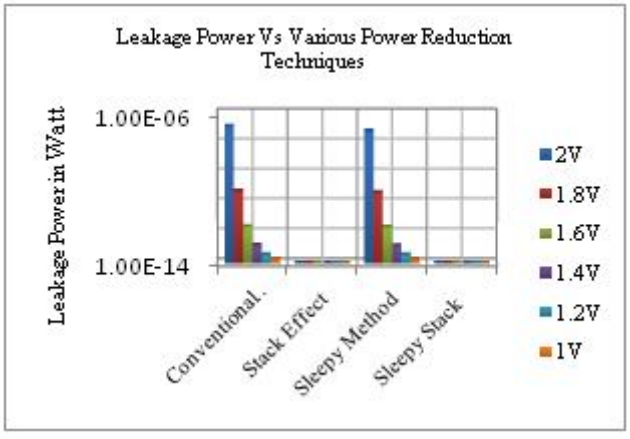

Figure 5. Leakage Power Vs Various Leakage Reduction Techniques

V. Conclusion

Various methods in reducing the leakage current components in a CMOS inverter are revisited in this paper. The different techniques applied here are mainly application based and used at 90nm technology. From the analysis, we can

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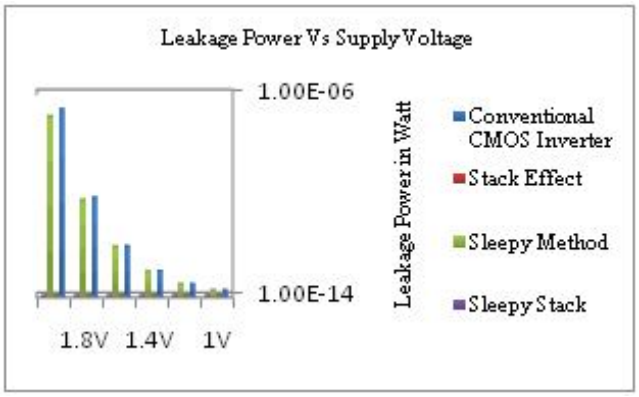

Figure 6. Power Dissipation Chart at Supply Voltages of 1V,1.2V,1.4V,1.6V,1.8V and 2.0V

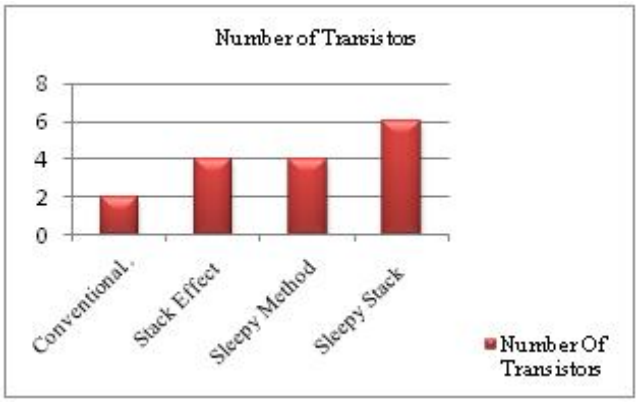

Figure 7. Graphical Representation of Transistor Count for Various Low Power Techniques

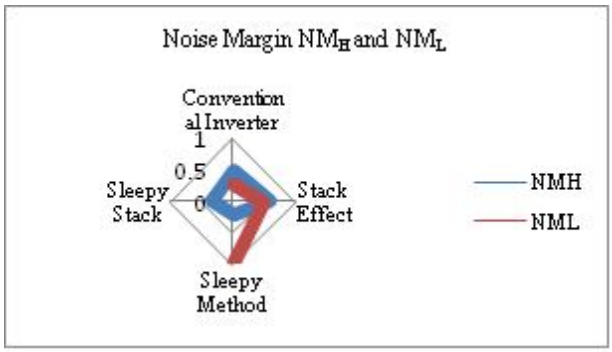

Figure 8. Noise Margin of Various Low-Power Techniques

conclude that stack and sleepy stack is a better technique in reducing power caused by leakage current. From all the techniques stack has the least leakage current and better noise margin with respect to others by using two extra transistors of half the W/L ratio than the conventional inverter. The sleepy stack is preferred over stack when we need to retain the state along with low power at the cost of two extra transistors. Further scope to this paper involves studying methods involving transistors of different threshold voltage in the logic.

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